



CLAIM AMENDMENTS

Please amend the claims as follows.

Please cancel claims 1-4 and 8-10, without prejudice.

AI 5. (Original) A reconfigurable computing chip comprising an on-chip configuration cache containing a multiplicity of stored configurations, wherein each configuration is identified by a unique off-chip address used to fetch that configuration.

6. (Currently amended) [The apparatus] The reconfigurable computing chip of Claim 5, where each configuration is compressed.

7. (Currently amended) [The apparatus] The reconfigurable computing chip of Claim 5, where the identification of the address is performed using contents-addressable memory.

Please add the following new claims:

11. (Currently Added) The reconfigurable computing chip of claim 5, wherein the on-chip configuration cache includes an compressed cache.

12. (Currently Added) The reconfigurable computing chip of claim 5, wherein the on-chip configuration cache includes a decompressed cache.

13. (Currently Added) The reconfigurable computing chip of claim 12, further comprising an active configuration plane configured from configuration content retrieved from the decompressed cache.

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14. (Currently added) The reconfigurable computing chip of claim 13, wherein the on-chip cache includes a compressed cache.

15. (Currently added) The reconfigurable computing chip of claim 14, wherein the configuration content in the decompressed cache is promoted from the decompressed cache.

16. (Currently added) A method of configuring a reconfigurable chip, the method comprising:
decompressing configuration content resident within an on-chip compressed cache; and
storing the decompressed configuration content in an on-chip decompressed cache from
which an active configuration plane is configured.

17. (Currently added) A method of configuring a reconfigurable chip according to claim 16,
further comprising:
configuring an active configuration plane of the reconfigurable chip from configuration
content in the on-chip decompressed cache.

18. (Currently added) A method of configuring a reconfigurable chip according to claim 17, the
element of configuring comprising:
decoding configuration content from the on-chip decompressed cache; and

applying configuration content to intersections of select rows and columns, including a multiplicity of such intersections for the same configuration content.

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end
19. (Currently added) A method of configuring a reconfigurable chip according to claim 18, the element of configuring further comprising:

changing at least a subset of a computing element's configuration;

holding fixed at least some of a storage element's configuration to implement data-in-place reconfiguration of the reconfigurable chip.

20. (Currently added) A system comprising:

a reconfigurable chip including an on-chip configuration cache containing a multiplicity of stored configurations, wherein each configuration is identified by a unique off-chip address used to fetch that configuration; and

an external storage, coupled with the reconfigurable chip, from which at least a subset of the multiplicity of stored configurations may be fetched.

21. (Currently added) A system according to claim 20, wherein each configuration is compressed.

22. (Currently added) A system according to claim 20, wherein the identification of the addresses is performed using content-addressable memory.
